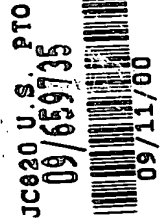


#4
CDS
NIT-83-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: Y. SASAKI et al
Serial No. 08/930,219
Filed: October 20, 1997

Group Art Unit: 2763
Examiner: H. Jones
For: METHOD FOR DESIGNING SEMICONDUCTOR
INTEGRATED CIRCUIT AND AUTOMATIC
DESIGNING DEVICE



INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
Washington, D.C. 20231

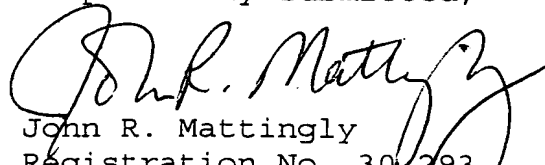
Sir:

In accordance with the duty of disclosure, the applicants inform the Examiner of the documents cited during prosecution of the parent application, Serial No. 08/930,219.

The above-referenced patent application is a continuation application of U.S. Application Serial No. 08/930,219, filed on October 20, 1997, from which priority is claimed under 35 U.S.C. § 120.

The applicants request the Examiner to initial and return a copy of the attached PTO-1449 form to indicate that the references have been considered.

Respectfully submitted,


John R. Mattingly
Registration No. 30,293
Attorney for Applicants

MATTINGLY, STANGER & MALUR
104 East Hume Avenue
Alexandria, Virginia 22301
(703) 684-1120
Date: September 11, 2000

FORM PTO-1449
(REV. 7-80)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.
NIT-83-02

SERIAL NO.

LIST OF DOCUMENTS CITED BY APPLICANT
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APPLICANT

Y. SASAKI et al

FILING DATE

9/11/00

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2763

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						YES	NO
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AS	INFORMATION PROCESSING SOCIETY OF JAPAN, PROCEEDINGS OF 1994 AUTUMN NATIONAL CONFERENCE, Vol. A, p. 64.
AT	PROCEEDINGS OF IEEE 1994 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1994, PP. 603-606.

EXAMINER

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AL	1-216622	08/30/89	Japanese Laid-Open Patent				
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AT	IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-22, No. 2, April 1987, "CMOS Differential Pass-Transistor Logic Design", Pasternak et al. pp. 216-222.

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		FILING DATE 9/11/00	GROUP 2763

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AT		

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	AP						<input type="checkbox"/>	<input type="checkbox"/>

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	AT		Fujita et al.; Automatic and semi-automatic verification of switch-level circuits with temporal logic and binary decision diagrams; ICCAD-90; pp. 38-41 11/90

EXAMINER

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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.